23. (New) The method of claim 19, further comprising:

during the refresh operation, reading the digital indication from the memory.

24. (New) The method of claim 19, further comprising:

during the refresh operation, latching the digital indication.

25. (New) The method of claim 19, wherein the refresh and frame update operations are associated with different rates.

26. (New) A method comprising:

providing capacitors, each capacitor being associated with a different pixel cell to maintain a terminal voltage of the associated pixel cell near a predetermined voltage;

providing first memory buffers, each first memory buffer being associated with a different one of the pixel cells and storing a first digital indication of the associated predetermined voltage;

providing a second memory separate from the first memory buffers to store second digital indications of updated voltages for the pixel cells;

during a frame update operation, communicating the second digital indications from the second memory to update the terminal voltages of the pixel cells; and

during a refresh operation, converting the first digital indications into analog voltages to update charges on the capacitors.

27. (New) The method of claim 26, wherein the second indications are not communicated from the second memory during the refresh operation.

28. (New) The method of claim 26, wherein the first memory buffers are localized to the different associated pixel cells and the second memory is a global memory associated with the pixel cells

29. (New) The method of claim 26, wherein the capacitors are associated with a row of pixels.

30. (New) The method of claim 26, wherein the memory buffers comprise a part of a static random access memory.

31. (New) The method of claim 26, further comprising:

during the refresh operation, reading the digital indications from the memory buffers.

32. (New) The method of claim 26, further comprising:

during the refresh operation, latching the digital indications.

33. (New) A light modulator cell comprising:

a pixel cell;

a capacitor to maintain a terminal voltage of the pixel cell near a predetermined voltage;

a first memory to store a first digital indication of the predetermined voltage;

a second memory separate from the first memory to store a second digital indication of an updated voltage for the pixel cell;

a circuit to during a frame update operation, communicate the second digital indication from the second memory to update the terminal voltage of the pixel cell; and

a digital-to-analog converter to convert the first digital indication into an analog voltage to update a charge on the capacitor during a refresh operation.

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34. (New) The light modulator cell of claim 33, wherein the circuit does not communicate the second indication from the second memory during the refresh operation.

35. (New) The light modulator cell of claim 34, wherein the refresh operation occurs at a different rate than the frame update operation.

36. (New) The light modulator cell of claim 33, wherein the memory comprises a static random access memory.

37. (New) The light modulator cell of claim 33, further comprising:

bit latches; and

sense amplifiers to communicate the digital indication from the memory to the bit latches during the refresh operation.

38. (New) The light modulator cell of claim 33, further comprising:

bit latches to latch the digital indication during the refresh operation.

39. (New) The light modulator cell of claim 33, wherein the memory further is updated with another digital indication of another predetermined voltage.

40. (New) A light modulator comprising:

pixel cells;

capacitors, each capacitor being associated with a different pixel cell to maintain a terminal voltage of the associated pixel cell near a predetermined voltage;

first memory buffers, each first memory buffer being associated with a different one of the pixel cells and storing a first digital indication of the associated predetermined voltage;

a second memory separate from the first memory buffers to store second digital indications of updated voltages for the pixel cells;

a circuit to during a frame update operation, communicate the second digital indications from the second memory to update the terminal voltages of the pixel cells; and

digital-to-analog converters to convert the first digital indications into analog voltages to update charges on the capacitors during a refresh operation.

41. (New) The light modulator of claim 40, wherein the refresh operations occurs at a different rate than the frame update operation.

42. (New) The light modulator of claim 40, wherein the circuit does not communicate the second digital indications from the second memory during the refresh operation.

43. (New) The light modulator of claim 40, wherein the capacitors are associated with a row of pixels.

44. (New) The light modulator of claim 40, wherein at least one of the memory buffers comprises a static random access memory.

The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0312US).

Respectfully submitted,

Date: September 25, 2002

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